FIRST OPERATION OF DSP-BASED CONTROLLER BOARD

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A DSP-based Industry Pack carrier board was used for the first time in the Control system of the high intensity proton accelerator facility. With this board we were able to meet the high requirements that had to be realized to perform the first beam tests with the UCN (Ultra Cold Neutron) kicker magnet. The carrier board operates in a VME crate independently of the IOC-CPU, controlling the equipment, like a power supply in this case. The on-board digital signal processor (DSP) monitors the power supply and also other operating conditions like the signals from the Run Permit System (MRPS). It will also produce signals to the MRPS when the equipment is ready to operate. This provides an additional level of security and reduces the workload of the IOC-CPU. These first tests proved the validity of this concept and gave confidence for the future applications, many of which are highly safety-critical

INTRODUCTION

The control system of the High Intensity Proton Accelerator Facility is in the process of being gradually upgraded to VME hardware. The main driving force behind is the need to replace magnet power supplies some of which are nearly 30 years old with new digitally controlled ones that also are more precise and stable. The new power supplies are based on an architecture where there is a serial point-to-point link between the power supply controller and the controller in a VME crate.

The existing magnet controls at the proton accelerators are based on an integrated controller ("Kombi") that handles the controls locally. To enable a seamless upgrade, the new VME hardware has to provide a functionality similar to the existing hardware.

The new VME hardware architecture is based on the extensive use of Industry Pack (IP) modules, small mezzanine cards that provide I/O functionality like an ADC, DAC, motor controller and so on. IP modules are mounted on a so-called carrier board. Normally the main CPU (Input/Output Controller, IOC) in the VME crate handles the I/O access, and the carrier board is just a passive element. However, an intelligent carrier board with an on-board CPU would have several advantages. The CPU can work independently of the main IOC, thus relieving the IOC of routine tasks. The processing does not depend on the availability of the main IOC, which helps to improve the availability of the system. Also it is possible to implement some signal processing functions on the board, which would otherwise take excessive amount of the resources of the main IOC.

The proton accelerator control system has also a sophisticated Run Permit system, based on hardware connections that constantly monitors the status of the hardware and in case of trouble switches off the beam before the high intensity beam damages beamline components. This system is also in the process of being upgraded. The present CAMAC modules will be replaced with IP modules with enhanced functionality. Although the new modules were not yet used in these tests, the functionality was emulated with the use of a simple binary I/O module, connected to the Run Permit System.

The UCN kicker beam test was the first real test of this hardware architecture at the proton accelerators, and in addition to testing the kicker hardware, was also a valuable test and proof of the feasibility of this approach.

THE DSP-BASED CARRIER BOARD

The newly developed IP carrier board (VICB8003) has already been presented in [1], so we just summarize the features here. The board has a Digital Signal Processor (DSP), with its own memory. The DSP can access the IP cards directly and can thus perform local processing of the data read from or to be written to the IP modules. The memory on the carrier board is dual-ported so the main IOC can access it in parallel with the DSP.

The carrier board has on-board Flash EPROM to store programs and data. The Flash can be programmed through a serial port or through the VME bus; whatever is more convenient for the software development and maintenance. The DSP boots directly from the Flash and requires thus no external interaction to start.

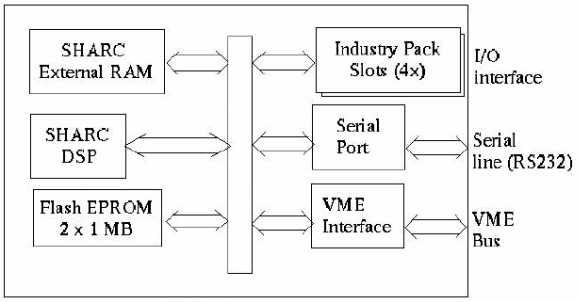

Fig. 1: Schematic diagram of the Carrier board (simplified).

The carrier board also has front panel connections for SHARC serial high-speed link ports that enable fast serial communication between two SHARC cards. With the links one can connect several carrier boards together to build chains of processors.

THE UCN KICKER CONTROL SYSTEM

A source of ultracold neutrons (UCN) is planned at PSI [2]. The neutrons will be created by diverting a small part of the proton beam to a spallation target. The diverting of the beam is done by a fast pulsed kicker magnet. To test the feasibility of the proposed source, the kicker magnet and a corresponding control system were built and installed into the beam transport line.

The system to control the UCN kicker during the tests consisted of the UCN kicker power supply plus connections to the run permit system (interlock). The power supply works in a pulsed mode, with the duty cycle (ratio of pulse/pause) being no more than 1 %. That is, for each triggered kick there must be a pause that is at least 100 times the length of the pulse.

The hardware required for the control system consists of a power supply controller IP module, a module to deliver a trigger pulse (optical) to the power supply and a binary I/O module to handle the connection to the Run Permit System.

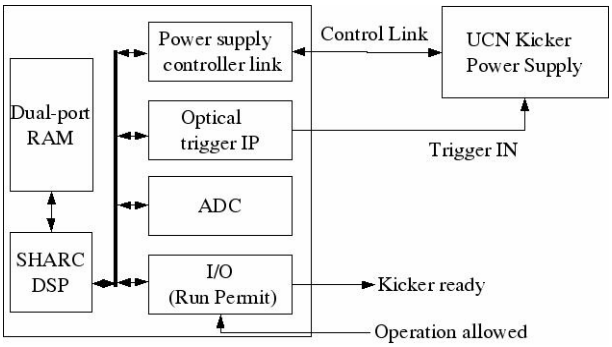

Fig. 2: The UCN Kicker control hardware.

The SHARC DSP on the carrier board executes a program that communicates with the power supply controller. The program sets and reads the corresponding setpoints for current and pulse length, reads the status information, handles commands like switching on and off of the power supply and so on. The program also monitors the status given through the run Permit System, and does not allow the power supply to be pulsed until the operating mode is correct. When the MRPS gives an ‘OK” status to the carrier board, the program allows the pulsing.

The control parameters, set points and readback values are held in the DPRAM of the carrier board, where the main IOC can access them. The parameters are defined as memory-mapped registers which resemble the register structure of the existing controllers whenever possible. The status information from the power supply consists of status codes, which are summarized as bits in a status register.

The control loop is executed with a frequency of about 10 kHz, meaning that the SHARC can interrogate all the relevant parameters of the power supply with this rate.

UCN KICKER TEST

The first beam test of the UCN kicker [3] was done in December 2002. The tests involved firing the kicker magnet and measuring the deflected beam parameters down the beam transfer line. For the control system we could verify that the carrier board and the related DSP software operated as expected, with essentially all the functionality needed for the final application. Some enhancements to the software remain to be done, but all in all the board and the software performed according to expectations. The board had been started before the tests while the power supply was switched off. When the power supply was turned on for the tests, the communications to the power supply were immediately restored and the control system started to function.

CONCLUSIONS

The tests for the UCN source kicker were successfully performed. The control system of the kicker was a first real field application of the newly developed carrier board with an on-board DSP. The board and the DSP program to control the UCN kicker performed well in these tests, verifying the plausibility of this approach. Further application of the board to control several more power supplies can be done by extending the software functionality to handle more power supplies and different functions. The kicker power supply is a special case and the normal magnets require some features that were not implemented yet.

This carrier board is planned to be used also in the Patient Safety System of the PROSCAN project, where multiple boards would run in a redundant configuration to enhance the reliability of the system.

Further applications can include preprocessing analog data, for example implementing a digital filter on a noisy input, or enhancing the performance of an ADC by using a suitable filter algorithm.

The test was short but nevertheless proved that the taken approach is feasible and gave us good experience for the further development of the hardware and software.

REFERENCES

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