NEW DEVELOPMENTS FOR THE SLS TIMING SYSTEM

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The SLS timing system has been in operation since the SLS commissioning started in July 2000. For time-resolved beamline experiments, some new requirements have emerged recently. These requirements can be fulfilled with the timing system, but required some enhancements like distribution of programmable frequency signals. The new features were implemented in the timing system firmware and initially tested during the year 2002.

INTRODUCTION

The task of the SLS timing system [1] is to synchronize the operation of the components of the SLS. The injection cycle, the beam diagnostic devices and so on operate according to synchronisation pulses from the timing system.

The timing system is based on a distribution of an event signal stream from one timing source to several receiving stations. The synchronisation events are encoded onto this signal and recovered at the end stations.

The system was primarily designed to meet the needs of the machine synchronisation, but was also foreseen to cover at least a majority of the synchronisation needs of the photon beam line experiments.

Needs that require some extensions to the system have arisen for the beam line experiments and for some applications for the machine control. The event system has some additional capacity that was not used so far. By enabling the use of this extra capacity, we can fulfill most of the new needs within the single system, and even simplify further the existing setup.

NEW TIMING REQUIREMENTS

A number of proposals for time-resolved studies at SLS beamlines have been made. These experiments typically require a special filling mode, either a single bunch or a hybrid fill, where in addition to a regular filling pattern an isolated single bunch is injected. To be able to resolve this single bunch one needs at minimum a beam revolution clock signal that is synchronized to a known bunch. In addition there are needs for subharmonics of this, like for instance triggering every tenth turn of the beam in the storage ring.

The most common way to create signals like these is by downconversion of the RF frequency with dedicated hardware. The resulting signals are then distributed with dedicated cables to the users. However, this kind of baseband signal distribution has a number of drawbacks; the cabling is expensive and the number of signals per cable is limited to one, the cables can pick up noise that reduces their precision and generating of these signals requires custom hardware that has to be built explicitly for this purpose.

At the SLS we can apply a different method. In the event system, the timing signals are encoded to a bitstream that is synchronized to the main RF. The bitstream is delivered to the end station and is received by an Event Receiver (EVR) module. The EVR locks to the incoming signal and recovers the original timing of the bitstream with a high precision. Clock signals that are generated at the source and multiplexed to the bitstream can be recovered at the end station without any additional cabling or electronics. Then one is not limited to only one signal but is able to select any one that is generated at the source, and the selection can be done by software on-line. And not only the clock signals but also all the other timing events like top-up warnings can be received.

IMPLEMENTATION

The internal logic of the timing signal source, the Event Generator (EVG), is based on a Field Programmable Logic Array (FPGA), which can be easily modified to add new functionality, as long at the capacity of the FPGA is not exceeded.

The EVG uses a subharmonic of the RF signal as its internal clock ($f_{RF}/5$). All the operation is thus synchronized to the RF. The event bitstream consists of 16-bit frames that are transmitted at 50 MHz frequency (or $f_{RF}/10$.) Half of this bandwidth, that is, 8 bits per each frame is used to transmit event codes; the other 8 bits have been defined as a “Distributed Bus”, where any externally generated signals, with a maximum frequency of 25 MHz can be distributed to all the receivers. This enables the distribution of any clock signal that is an even subharmonic of $f_{RF}/10$. For instance, the storage ring revolution clock (1.04167 MHz, 960 ns cycle) can be generated by dividing the 50 Hz frequency by 48.

Instead of using external hardware to generate the clock signals, 8 frequency dividers were added to the Event Generator FPGA firmware. It is possible to selectively multiplex any (or all) of the frequency divider outputs to the Distributed Bus bits. The counters also have a synchronized reset so that the clock signals can be synchronized with the injection and are then always at a constant phase with respect to the filling pattern of the machine. The signals are then recovered from the bitstream by the EVR, and can be used to trigger subsequent electronics at the experiment.

These new features can be used with the existing Event Generator cards, by simply downloading the new firmware to the cards.

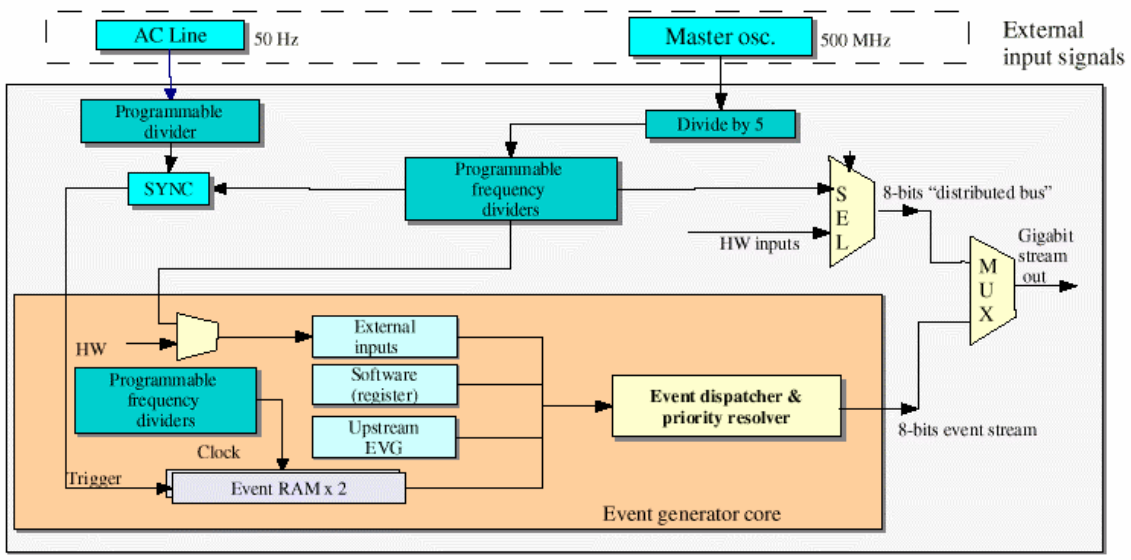

Fig. 1: Block diagram of the new EVG-Plus card.

At the same time, we realized that with the new capabilities and a couple of hardware enhancements, it would be possible to further simplify the timing system. With the added frequency dividers it is possible to generate all the required timing fiducials within the EVG card, if the possibility to synchronize with the 50 Hz AC line would be built in. In addition, a prescaler would enable the EVG to accept directly the 500 Hz RF signal. Since spare modules needed anyway to be ordered, a new version was built with these enhancements. With the new version, all the timing references can be generated internally without requiring any additional external components.

NEW CAPABILITIES

The built-in frequency dividers give us the possibility to deliver several clock signals over a single cable, under software control so that the signals can be changed according to the existing needs and the machine configuration. There is no need to build special-purpose electronics to generate these signals. Some equipment that was used only to generate a fixed frequency clock signal can be replaced by the internal frequency generator. Some electronics that was built in-house and has a limited number of spares is not necessarily needed anymore, easing the long-term maintenance.

In addition to distributing the clock signals the dividers can be programmed to trigger regular events also. For events one can use the delay and pulse width setting facilities, triggering of software processing and so on. This is potentially useful for certain types of machine diagnostics where one could with precise frequency repeatedly trigger measurements and data collection, globally synchronized but still easily configurable via software.

CONCLUSIONS

A number of additional features have been implemented in the SLS timing system hardware. These additions enable flexible distribution of clock signals to all locations where timing is needed, using only a single optical fiber that is in most cases already available. The frequencies can be configured with software and received at the end stations according to the user needs.

In addition, a number of enhancements were built to a new version of event generator cards. The cards now have direct RF and AC line frequency inputs. With these cards the timing distribution system can essentially be simplified into a single event generator card, which makes the system simple and the maintenance easy.

What might be even more important, the new modules make it simple to build branches where an additional event generator is added in cascade. This would enable a very sophisticated timing arrangement for an experiment, where all the upstream (machine) timing is available, and in addition the experiment can use the cascaded event generator to generate its own synchronized operating sequence.

REFERENCES

[1] T. Korhonen, M. Heiniger *The Timing System of the Swiss Light Source*, Proc. ICALEPCS'01 (2001).

[2] *Event System User's Guide*, Micro-Research, Finland, (revised) December 2002.