CAPABILITIES OF THE ELETTRA/SLS MULTI BUNCH FEEDBACK ELECTRONICS

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Following the cessation in the production of the commercial ADC/DAC boards adopted by the ELETTRA/SLS digital multi-bunch feedback systems, a new family of 500 MS/s data conversion boards with an 8 bit resolution has been developed. The ADC and DAC circuits are separate modules containing analog and digital electronics providing a data rate of 500 MSample/sec using 250 MHz DDR clocking techniques. The following stage being a common design to both ADC and DAC reduces the data rate to 125 MS/sec, allows data recording and play back using on board RAM and allows freely programmable multiplexing/ demultiplexing up to ratios of one to twelve. The digital data streams flow via Front Panel Digital Ports (FPDP). Special attention was paid to low system latencies ensuring a high feedback efficiency. Apart from lab tests, we report on feedback system test and describe additional hardware applications.

INTRODUCTION

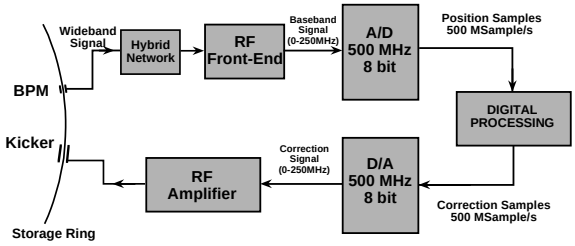

Fig. 1: System Layout for the transverse multi bunch feedback

The ELETTRA/SLS Multi-Bunch Feedback System is a wide band feedback correcting the positions of individual bunches, spaced 2 ns apart (Figure 1). Wide band position signals coming from button type BPMs get converted to baseband (DC-250 MHz), followed by sampling with a fast 8 bit, 500 MS/s Analog to Digital Converter (ADC). A digital filter calculates correction kicks, which are getting reconverted via 8 bit, 500 MS/s Digital to Analog Converter (DAC). For the transverse feedback, the signals are directly fed via broad band power amplifiers and strip line kickers to the beam, in the longitudinal plane, a Lower Single Side Band (LSSB) modulator mixes the signals up to the 1.25-1.5 GHz band, where they get amplified and fed to a longitudinal kicker [1] [2].

The digital filter (Fig. 2) consists of the ADC itself, which is followed by a first one to four demultiplexing stage. A second one to six demultiplexing reduces the data rate to approximately 20 MS/s, The six Front Panel Data Ports (FPDP) each feed a quad processor board containing TI-TMS320C6201 Digital Signal Processors (DSP). Three processors per board concurrently calculate the correction kicks, whereas one DSP takes all the data from the FPDP port and is used for on-line beam diagnostics.

The system described has been shown to work (e.g. [1]) and two systems are in routine operation on the vertical and horizontal planes at ELETTRA. A show stopper in setting up a feedback for all planes proved to be the cessation of production of the ADC and DAC boards, which were planned to be used. Following that, it was decided to launch our own development of ADC and DAC boards, at the same time trying to improve on the suitability for feedback and other accelerator applications. The main specifications of the boards are given in table 1.

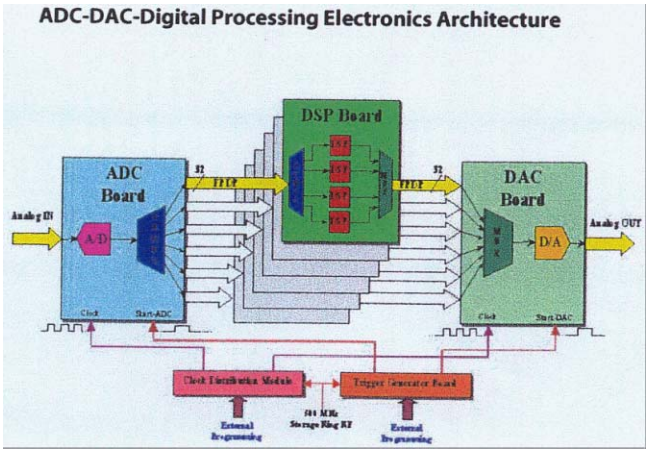

Fig. 2: Digital filter structure

ELECTRONICS

The similarities in the functionalities of ADC and DAC boards shows up also in the layouts in figures 3 and 4 and was exploited to simplify the development process. Both boards consist of three functional blocks, the first being a dedicated mezzanine in 50 Ω matched technology and containing the pure ADC or DAC circuitry. Common to both layouts is the main board containing the VME interface, a Xilinx Virtex II FPGA and (as of now) eight MBytes of ZBT RAM. The third block, also common in terms of hardware to both ADC and DAC, is the FPDP connector card. For both main board and FPDP board, only the FPGA firmware and the mezzanine card (ADC or DAC) attached determine the difference in the functionality.

Sampling Rate	200-500 MHz
Resolution	8 bits
Input Impedance	50 Ω
Coupling	AC
Analog Bandwidth (3 dB)	5kHz - 500 MHz
In-band Phase Rotation	$< 10^o$
Input Level(ADC)	0 dBm
Output Level(DAC)	6 dBm
Signal/Noise + Distortion Ratio	
(Total Dynamic Distortion)	$>$ 40dB
External Clock	Sine Wave/DECL
Clock Programmable Shift	Range $>$ 2ns, steps $<$ 100 ps
External Trigger	DECL
Total Jitter from Clock Input to Analog I/O:	$<$ 10 ps
VME interface	VME64x compatible A32/D32 (base address geographic or switch selectable)
FPDP Interface	ANSI/VITA 17 Single Ended TTL, 80 pin connector
Number of FPDP Ports	1 to 12
Memory Size	8 MByte

Tab. 1: Main ADC and DAC specifications

The ADC communicates with the main board at a 500 MS/s data rate via the LVDS bus. In the main board FPGA, the eight bit data is demultiplexed with a ratio of one to four to produce a 32 bit wide internal data rate at 125 MHz. The data passes a Gray to Binary decoder and a 2 ways data redirector, which may send the data either to the FPDP board for further demultiplexing or the ZBT memory, which is configured as ring memory, or to both. For hardware debugging purposes, the ZBT memory can also be written via the VME interface and used to generate data streams at the FPDP ports. The FPDP board takes the 125 MS/s data from the main board and does an additional demultiplexing with a programmable ratio of one to five to one to twelve, which are sent out to the FPDP ports. For demultiplexing ratios in the excess of 6 an additional board is necessary purely to carry the required connectors. The board can be triggered either via a software trigger or an external DECL trigger signal. A photo of the main board is shown in figure 5.

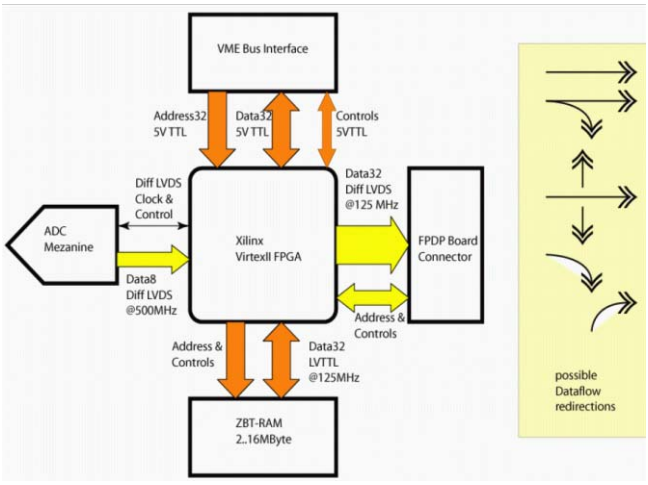

Fig. 3: Layout and data flux for the ADC board

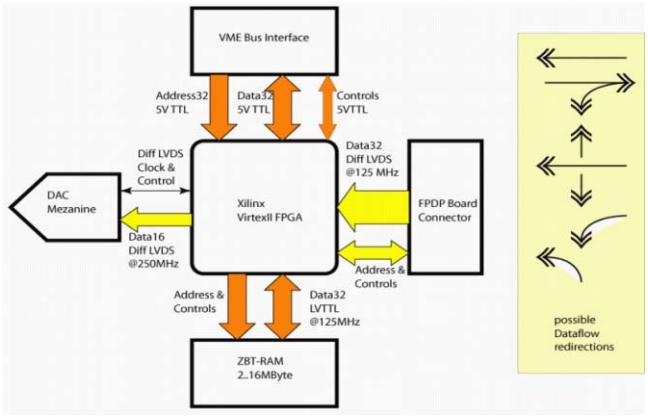

Fig. 4: Layout and data flux for the DAC board

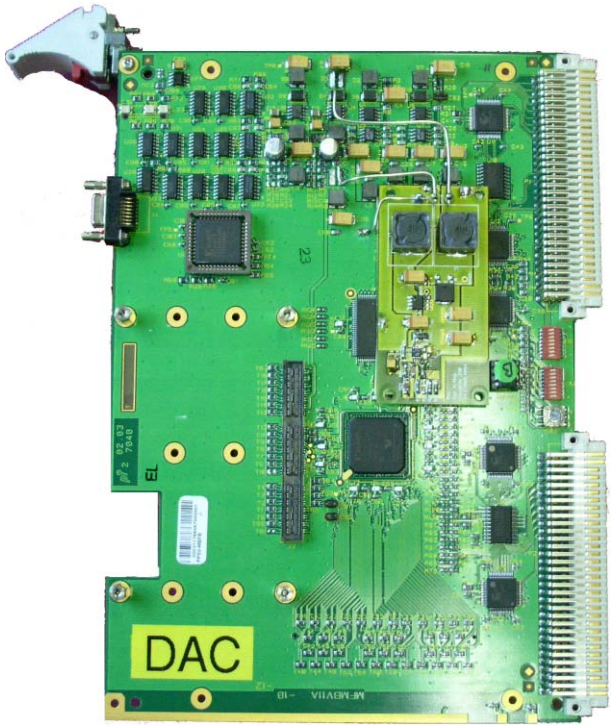

Fig. 5: Photo of ADC/DAC main board.

The DAC works in the reverse manner. The FPDP board, being triggered via the Data Valid (DVALID) line of the FPDP ports, multiplexes the input data into a 32 bit 125 MS/s data stream for the main board FPGA, where it is buffered into an internal FIFO register. A START_DAC trigger (external DECL or software) launches the second one to four multiplexing stage in order to produce the 500 MS/s data for the DAC circuit. Analog to the ADC, a 2 ways data redirector is incorporated into the chip, which allows storing FPDP input into the internal RAM and even using the DAC for data playback, where a signal written into the ZBT RAM is fed to the DAC.

An important parameter determining the efficiency of any feedback application is the latency of the data throughput, which was reduced to a total of 88 ns for ADC and DAC board combined.

BEAM TESTS

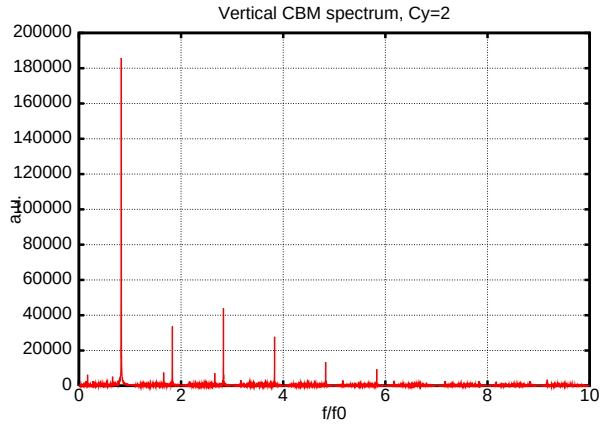

Fig. 6: Vertical coupled bunch mode spectrum, 75 mA beam current with all buckets filled, vertical chromaticity set at three times the standard value.

Laboratory tests have been done for the ADC and DAC board and have shown the correct function of both systems. In work at the moment is the last iteration for the firmware program of the FPGA used allowing among other hardware triggering of the data aquisition. With the ADC board, a first commissioning run for the front end part of the transverse multi bunch feedback has been done. The system consists of the RF front end, the new ADC board used with a demultiplexing ratio of one to six connected to the six DSP board. Equally included was another new development, a four channel 500 MHz DECL clock generator/shifter. Without the DAC, the system was used as a passive diagnostic device, reading out bunch by bunch vertical position data via the diagnostics DSPs.

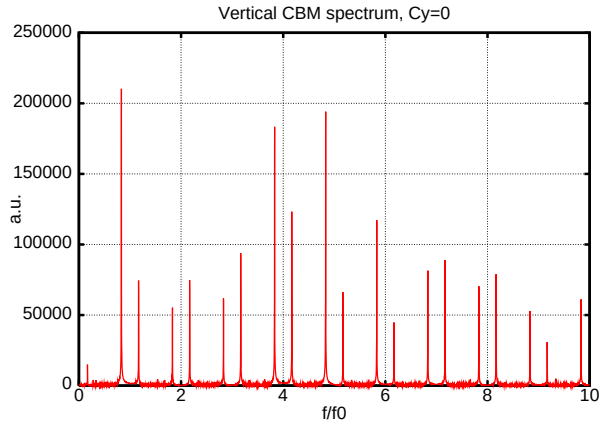

Fig. 7: Vertical coupled bunch mode spectrum, 75 mA beam current with all buckets filled, vertical chromaticity set to standard value.

For testing, we used a non standard homogeneous fill without any gap with an average current of 75 mA. Since there is no gap in the fill pattern, coupled bunch modes due to daisy chain like effects as resistive wakes and ions will show up quite clearly despite the comparatively low current. Varying the chromaticity of the ring produces a mix of combinations of these effects.

With a high chromaticity setting just below the stability threshold at three times the nominal value, the spectrum in figure 6 was obtained, showing high peaks a $Q = -1, -2, -3 \ldots + Q_y$, $Q_y = 0.17$ typical of an instability dominated by resistive wakes. Lowering the vertical chromaticity further to the nominal value leads the CBM spectrum in figure 7, where resistive wall instabilities are still recognizable, but the beam motion is dominated by other effects, probably of the ion type.

OUTLOOK

As the complete system becomes operational in the next months, the main application for the new boards will be to commission and get into operation the bunch by bunch feedback systems for all three planes at SLS and for the longitudinal plane at ELETTRA (Two systems are in operation for now.). Extremely interesting is the strongly reduced latency of the new development in comparison to the original boards, which will allow to reduce the latency of the overall digital filter by one whole bunch circulation period (960 ns in the case of SLS), so that higher efficiency and better performance can be expected.

Another system planned now is a bunch by bunch current feedback, optimizing the behavior of the SLS top up system [3]. The feedback RF front end together with a stand alone ADC board is going to be used to read out the sum signal of a BPM pickup. This information will be used for selective refilling of empty buckets in order to have a highly controllable fill pattern.

A third application will be taking bunch by bunch data from the wide band BPM and microwave front end installed in the SLS storage ring, which will allow to measure intra bunch charge distributions for individual bunches within a multi bunch filling [4].

REFERENCES

[1] D. Bulfone et al, *The ELETTRA Digital Multi-Bunch Feedback Systems,* proc. of EPAC 2002, Paris, France, June 2002.

[2] M. Dehler, *Kicker design for the ELETTRA/SLS longitudinal feedback,* proc. of EPAC 2002, Paris, France, June 2002.

[3] T. Korhonen, B. Kalantari, personal communication.

[4] M. Dehler, *Microwave measurement of intra bunch charge distributions,* proc. of the DIPAC 2003, Mainz, Germany, 2003.