# INTRODUCING THE "VME GENERIC PMC CARRIER BOARD": A MODULAR APPROACH FOR BEAM INSTRUMENTATION AT PSI

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*The large variety of measurement applications for the PSI accelerator diagnostics section leads to a modular approach in electronics design. The backbone of such a concept is the so called "VME generic PMC carrier board" (VPC), which is acting as a highly flexible data processing and communication unit between customized front end electronics and the standardized VME control system. The VPC specifications and design concept, which was elaborated with in the DACSY initiative at PSI is presented and a short status of the project is given in this paper.*

## INTRODUCTION

The acceptance of the VME64x standard [1] as a common HW-platform for all GFA accelerators at PSI, motivates a modular approach in electronics design. The so called "VME generic PMC carrier board" (VPC) [2] represents the backbone of such a concept, acting as a highly flexible data processing and communication module between customized front end electronics and the standardized VME-based control system. It is designed to serve a large variety of measurement and data-processing applications, with special emphasis on high speed VME data acquisition, high speed number crunching and real time data processing. The presentation of the VPC design within the DACSY (**D**ata **A**cquisition and **C**ontrol **SY**stem support group) initiative of PSI has already lead to a wide interest in the board, proving the validity of such a generic and flexible HW solution. Over 400 VPC boards will be used in various experiments throughout PSI such as accelerator diagnostics, the MEG experiment [3] as well as instrumentation and control system applications [4].

## MODULAR ELECTRONIC DESIGN

A considerable number of new projects within the PSI accelerator divisions such as Femto pulse slicing [5], LEG [6] and PROSCAN [7] as well as the continuous electronics upgrade for the proton cyclotron and improvement of SLS beam performance require a large variety of diagnostics systems in the near future. Therefore, a modular approach in electronics design was chosen, where the acquisition of monitor signals is done in customized front end electronics, while data processing, analysis and transfer to the control system or to (fast) feedback applications is accomplished by a fast and flexible communication unit.

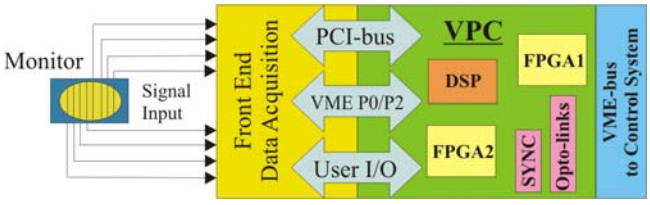


**Fig. 1:** *Schematic view of modular electronics design for future electron and proton accelerator diagnostics.*

Figure 1 illustrates schematically the main blocks of future diagnostic systems based on the VPC board. The possibility of interfacing different kinds of front end data acquisition modules through front panel PMC mezzanine access or VME backplane P0 and P2 user I/Os shows the flexibility of the VPC as a central communication unit. Two field programmable gate arrays (FPGA) with embedded PowerPC™ processors form the kernel of the board. A digital signal processor (DSP) is available for onboard data analysis and data reduction in floating point format. The VPC board can be equipped with a wide range of commercial PMC mezzanine boards that use the standard 66 MHz PCI system bus protocol. Using one of the FPGAs as VME-PCI bridge also allows in-house developments of PMC mezzanines with user defined protocols instead of PCI. Two optional bidirectional optical Gigabit links based on the RocketIO™ protocol may be used to acquire or distribute data, e.g. for distributed feedback applications. VPC boards can be synchronized with each other by trigger inputs. FPGA firmware customisation can be made by the user independently from a generic firmware package in FPGA1 ("VME/PCI FPGA") that handles the data transfer between VME, PCI, DSP, flash memory and the application-dependent firmware in FPGA2 ("I/O FPGA"). Full access from FPGAs to all user I/O pins on the VME bus (P2 and P0 connectors) and on the PMC bus provides full hardware configuration flexibility. The so called "live insertion" feature allows insertion or removal of boards without switching VME crates off.

## VPC SPECIFICATIONS

The final specifications of the VPC board have been worked out within the DACSY initiative. The design and layout as well as the provision of the fundamental firmware package for the systems FPGA will be completed by the PSI accelerator diagnostics group, while each user has the possibility to interface his specific hardware independently by programming the I/O FPGA. The following list summarizes the main features of the VPC board:

- VME 64x form factor (6HE/3TE)
- Live insertion
- 2 PMC mezzanine slots (PCI 66 MHz, 64bit)
- 2 Virtex2Pro™ FPGAs with two embedded PowerPC™ each

- 1 Sharc™ DSP with 3Mbyte SRAM
- Access from I/O FPGA to all VME P0 and P2 user IOs (up to 200) and PMC user IOs (64 per PMC)
- Connector for test and programming access
- 2 optional fiber optics transceivers (full duplex) for external communication with 2.125 GBd
- High-speed internal differential interconnections
- Full user access to FPGA firmware
- Firmware debugging by ACE controller and JTAG, ChipScope™, Windrivers Vision Probe or Agilent Trace Port Analyser.
- 8 Signal lines available on front panel connector for user defined signals (Trigger, Gate, etc…).

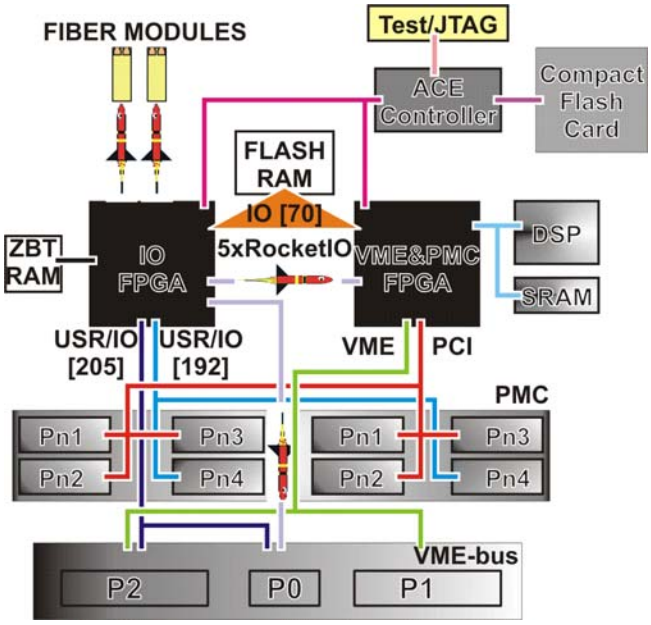


**FIG.2:** *Schematic layout of the VPC board, visualizing its modules and their electrical interconnections [8]*

The full flexibility of the VPC board can only be achieved through a generic VME/PCI FPGA firmware package, which is provided by the VPC design team. Since the development time for such highly complex firmware should not be underestimated, a modular on-chip bus concept was chosen, which allows gradual firmware enhancements according to the growing requirements of the VPC users [9]. The generic VME bus interface firmware enables the unification of low level control system software for different VPC applications, e.g. by using a C++ base class for generic VPC board features and derived classes for application specific VPC features.

The use of the high, in-house hardware and firmware design competence keeps all components of the system under control and minimizes the response time for support of the users and possible requests for modifications and further upgrades.

## STATUS AND OUTLOOK

The design and layout of the VPC board has been completed end of January 2004. First prototypes are expected to be available for hardware functionality tests until mid of March 2004. Assuming successful prototype tests using a first, fundamental firmware package a second iteration of 10-15 pieces will be produced until the end of April for integration tests in the lab. A first serial production of around 250 pieces for PROSCAN and MEG projects will be available in September 2004. The generic FPGA firmware package is well under development, including application examples for VME, DSP and PCI access as well as user I/O integration.

The main applications of the VPC board for PSI accelerator diagnostics in 2004/2005 will be a bunch pattern measurement for the SLS storage ring, the replacement of the DSP boards in the SLS booster synchrotron and a new, improved electronics for the proton cyclotron beam position monitors.

The participation of the PSI accelerator diagnostics section in the European coordinated accelerator research (CARE) program [10] and the European X-FEL project allows the test of VPC board based systems for the digital RF control and fast electron beam stabilization at the TESLA VUV FEL [11].

## REFERENCES

[1] American National Standard for VME64 ANSI/VITA 1-1994.

[2] P. Pollet et al., *Generic VME PMC Carrier Board Specifications.*

[3] http://meg.web.psi.ch/ - the MEG (μ-e-γ) home page.

[4] T. Korhonen, private communications.

[5] G. Ingold et al., *Sub-Picosecond Optical Pulses at the SLS Storage Ring*, PAC'01, Chicago, Illinois, June 2001.

[6] http://leg.web.psi.ch/ - web-page of the LEG (low emittance gun) project.

[7] http://proscan.web.psi.ch/ - the PROSCAN home page.

[8] P. Pollet et al., *VME Generic PMC Carrier Board,* Preliminary Datasheet Draft V1.1.

[9] B. Keil et al., *Generic VME PMC Carrier Board FPGA Firmware Specification*, Rev. 1.2.

[10] http://esgard.lal.in2p3.fr/ - link to the ESGARD and CARE web-page.

[11] http://tesla.desy.de/ - link to the TESLA test facility web-page.