STATUS AND PERSPECTIVES OF THE GENERIC VME PMC CARRIER BOARD (VPC)

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Rapid progress in digital electronics allows the digitisation of monitor signals at a very early stage of the signal processing chain, providing optimum performance and maximum flexibility for today's accelerator instrumentation. While the analog front-ends of such systems are usually specific for each monitor type, the subsequent digital part of the processing chain can be unified for many different measurement tasks. The "generic VME PMC Carrier board" (VPC) was developed within the PSI DACSY initiative [1] to achieve this unification for the PSI electron and proton accelerator diagnostics and fast data acquisition and feedback systems. This report gives an overview of the VPC hardware and firmware architecture and of present and future applications of the board, such as digital beam position (DBPM) and profile monitors for PSI proton accelerators, data acquisition and processing for the PSI "MEG" muon decay experiment, and the integration of photon BPMs into the SLS fast orbit feedback (FOFB).

INTRODUCTION

A significant number of new projects and cooperations in the PSI diagnostics section for proton, electron, photon and muon beam instrumentation and feedback systems motivated a modular design approach for the required monitor/detector electronics, with customised analog front-ends for each project, and the "VPC" VME64x board as common digital back-end for all projects. Rapid progress in digital electronics and FPGA (Field Programmable Gate Array) technology allows the digitisation of monitor signals at a very early stage of the signal processing chain, with functions like filters, mixers etc. being implemented digitally in FPGAs or microprocessors rather than with analog components or dedicated ASICs. This allows the design of flexible high-performance beam instrumentation systems with reconfigurable "intelligent" monitor electronics that can relieve the higher control system levels from tasks like data analysis, fit routines, feedback calculations, or the exchange of data and synchronisation signals between different boards for distributed feedbacks.

DESIGN STRATEGY

In the last decades the ongoing progress in IC integration enabled the reduction of the integration level for the digital part of complex monitor and feedback systems from crate level (e.g. a crate with several VMEbus boards) to board level (one VMEbus board with a large number of ASICs) and finally to chip level, where components like processors, RAM, buses, gigabit serialisers/deserialisers, clock generators, RS232 interfaces and application-specific modules like filters and detector interfaces can be integrated on a single FPGA. By choosing this "system-on-a-chip" (SOC) approach for the VPC board that uses Xilinx Virtex2Pro FPGAs, the number of other components on the VPC board could be reduced to connectors etc. and a minimum number of ICs that are not (yet) integrated in FPGAs, like larger amounts of RAM, transceivers for VMEbus and fibre optics, and non-volatile memory for FPGA configuration and boot software (Fig. 1). By shifting the system complexity from hardware to FPGA firmware and software that is written in portable languages like VHDL and C/C++, the dependence on special ICs and their future availability is minimised. Furthermore, the reconfigurability of SOCs allows the use of the VPC for a large variety of different applications and enables upgrades and even complete changes of the system architecture of an SOC within minutes by remote firmware upgrades. A modular generic approach for VHDL firmware and C/C++ software allows the re-use of modules for future designs and future FPGA generations and successors of the VPC board with little effort, thus maximising the synergy effects of present and future VPC applications at PSI.

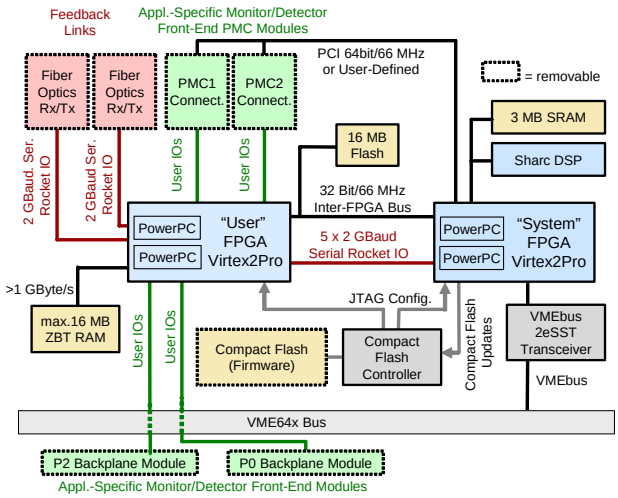

Fig. 1: Block diagram of the VPC board hardware.

HARDWARE ARCHITECTURE

Fig. 1 shows the main hardware components of the VPC board (see Ref. [1] for more technical details). The core of the VME64x board consists of two Virtex2Pro FPGAs with two on-chip PowerPC processors each, a floating point DSP and RAM. The FPGAs can acquire and process measurement data from two application-dependent PMC mezzanine modules or VMEbus P0/P2 backplane modules. Two optional SFP fibre optics transceivers or Ethernet transceivers may also be used to acquire or distribute measurement data at up to 2.125 Gbaud full duplex.

FIRMWARE ARCHITECTURE

Fig. 2 shows the modular structure of the generic System FPGA firmware that is common to all VPC applications. VMEbus, PCI (or user-defined) bus, User FPGA interface, DSP and compact flash controller are connected to an on-chip bus by suitable VHDL modules. So far the modules that are required for the first applications have been implemented (solid boxes). Additional modules (dotted boxes) will be added as required by future VPC applications. Fig. 3 shows a typical structure of the application-dependent User FPGA firmware. The interface to the monitor/detector front-end is usually written in VHDL, which allows high-speed parallel data processing and data decimation. The resulting lower data rate can be handled by the PPCs to perform high-level data analysis (fit routines etc.) in C/C++ code. The results can be transferred to the control system via VMEbus, to other VPC boards via fibre links, or to the DSP that has 10 times more floating point power than the PPCs.

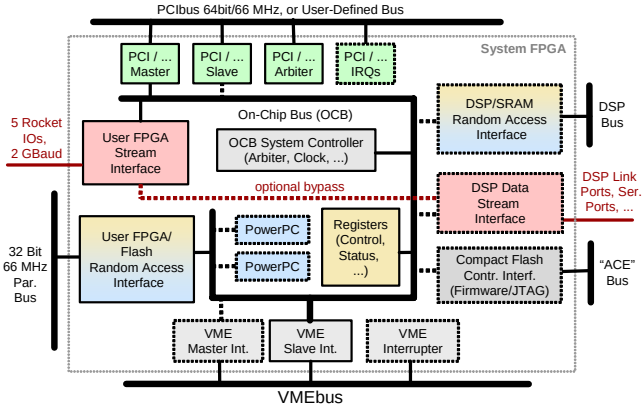

Fig. 2: Block diagram of the generic "System FPGA" firmware that is common to all VPC applications.

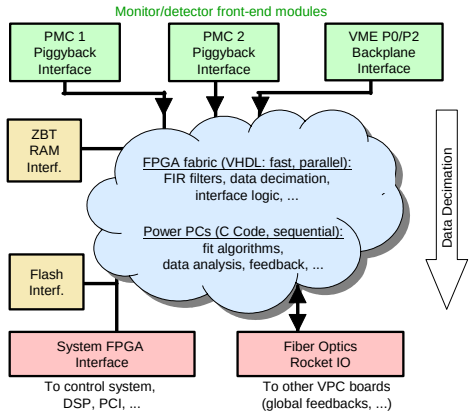

Fig. 3: Schematic diagram of the application-dependent "User FPGA" firmware of the VPC.

VPC APPLICATIONS IN 2004/2005

VPC prototypes are available to users since May 2004, including System FPGA firmware with the features required for the first applications, and example firmware for the User FPGA.

In August 2004, a 16-channel 4 GSa/s waveform digitiser PMC developed by S. Ritt for the detector readout of the PSI "MEG" muon decay experiment was successfully tested on the VPC in the lab, with a first User FPGA firmware version that allowed VMEbus readout of the waveforms, adjustment of the sample rate, etc. The first real particle (pion) decays were successfully measured with the VPC/PMC during a first test shift in October 2004.

In September/October 2004, the "LogIV32" (VME-P2) and "LogIV 4x4" (VME-P0) front-end electronics modules for the PROSCAN proton beam profile measurement [2] were successfully tested with the VPC in the lab, with a "beam profile simulator" box instead of the real profile monitor. While the first firmware version for these tests only provided basic functions like ADC waveform storage, VME readout, ADC sample rate adjustment etc., the final firmware will also use the PPCs on the User FPGA to analyse the beam profile, calculate the beam size and position, provide interlock signals, etc.

In September/October 2004, the communication between the VPC and the VME-P2 transition module for the new digital BPMs (DBPMs) for the PSI proton accelerators [2] was successfully tested, using externally developed User FPGA firmware that allowed basic hardware tests. The final firmware version for the DBPMs has a different structure that is based on the LogIV firmware, with a common part of more than 70%. This "generic" approach for parts of the User FPGA firmware significantly reduces the development time and simplifies maintenance, future extensions and control system interfacing not only for LogIV and DBPMs, but also for future applications.

An automatic test system for the VPC has been developed in 2004 for simple and quick tests and quality control of the several hundred VPCs that will be built in 2005/2006.

In 2005, the VPC will be used to integrate photon BPMs into the SLS FOFB, using the gigabit fibre optics links of the VPC for data transfer to the FOFB, and a newly developed VME-P2 module for the VPC to digitise the currents of the photon BPM blades.

FUTURE APPLICATIONS AND OUTLOOK

The VPC board and its FPGA firmware and software may also serve as a platform for future projects such as an upgrade of the SLS BPM and FOFB system, RF control and fast bunch-to-bunch feedbacks for VUV- and X-ray FELs at DESY and PSI, diagnostics for the SLS FEMTO and PSI LEG projects, and for an upgrade of the SLS multibunch-feedback.

REFERENCES

[1] http://dacsy.web.psi.ch/Projects

[2] P.A. Duperrex et al., *New VME-based electronics for proscan diagnostics*, PSI Scientific and Technical Report 2003, Volume VI.